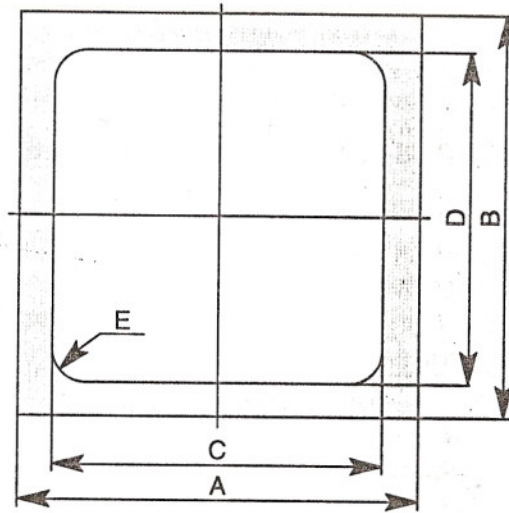




# Sierra Components, Inc.

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Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.



**Topside Metal: Al**  
**Backside: Ti/Ni/Ag**  
**Backside Potential: Cathode**  
**Mask Ref: Issue 1**  
**Bond Pads: .301" x .031"**

**APPROVED BY: CD**  
**MFG: Ixys**

**DIE SIZE: .195" x .341"**  
**THICKNESS: .016"**

**DATE: 7/24/02**  
**P/N: DWEP55-06**

DG 10.1.2  
Rev A 3-4-99